

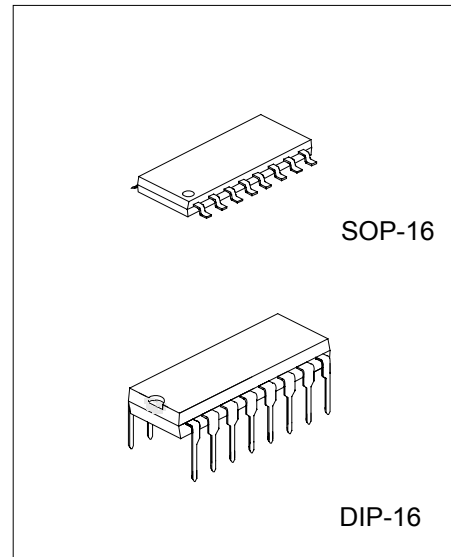
ANALOG MULTIPLEXERS /DEMULTIPLEXERS

DESCRIPTION

The UTC 4052 analog multiplexers is digitally –controlled analog switch. The device feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

FEATURES

- *Triple Diode Protection on Control Inputs
- *Switch Function is Break Before Make
- *Supply Voltage Range=3.0 Vdc to 18 Vdc
- *Analog Voltage Range(VDD-VEE)=3.0 to 18V
Note:VEE must be \leq Vss
- *Linearized Transfer Characterisitics
- *Low-noise-12nV/ $\sqrt{\text{Cycle}}$, $f \geq 1.0\text{kHz}$ Typical

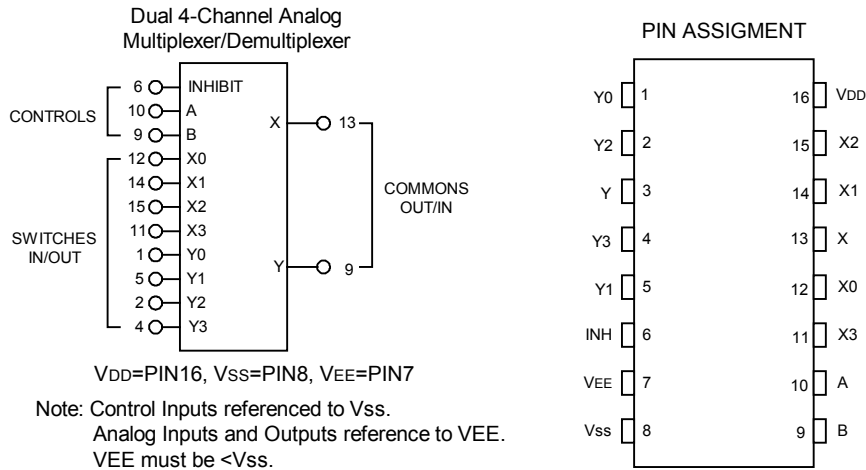


ABSOLUTE MAXIMUM RATINGS*1

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage (Referenced to VEE, Vss \geq VEE)	VDD	-0.5 ~ +18.0	V
Input or Output Voltage (DC or Transient) (Referenced to Vss for Control Inputs and VEE for switch I/O)	Vin, Vout	-0.5 ~ VDD+0.5	V
Input Current (DC or Transient) per Control Pin	Iin	± 10	mA
Switch Through Current	Isw	± 25	mA
Power Dissipation *2	PD	700	mW
DIP-16		500	
Ambient Temperature Range	TA	-55 ~ +125	$^{\circ}\text{C}$
Storage Temperature Range	Tstg	-65 ~ +150	$^{\circ}\text{C}$
Lead Temperature (8-Second Soldering)	TLEAD	260	$^{\circ}\text{C}$

*1. Maximum Ratings are those values beyond which damage to the device may occur.

*2. Temperature Derating : 7.0 mW/ $^{\circ}\text{C}$ From 65 $^{\circ}\text{C}$ ~ 125 $^{\circ}\text{C}$



ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	-55°C		25°C			125°C		UNIT
			MIN	MAX	MIN	TYP ³	MAX	MIN	MAX	
SUPPLY REQUIREMENTS (Voltages Referenced to VEE)										
Power Current Per Range	VDD	VDD-3.0 ≥ Vss ≥ VEE	3.0	18	3.0		18	3.0	18	V
Quiescent Current Per Package	IDD	Control Inputs: Vin=Vss or VDD, Switch I/O : VEE ≤ VIO ≤ VDD, and ΔVswitch ≤ 500mV ⁴ VDD=5.0V VDD=10V VDD=15V		5.0 10 20		0.005 0.010 0.015	5.0 10 20		150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	ID(AV)	TA=25°C only (The channel component, (Vin-Vout) /Ron, is not included.) VDD=5.0V VDD=10V VDD=15V	Typical			(0.07μA/kHz)f+IDD (0.20μA/kHz)f+IDD (0.36μA/kHz)f+IDD				μA
CONTROL INPUTS-INHIBIT, A, B, C (Voltages Referenced to Vss)										
Low-Level Input Voltage	VIL	Ron=per spec, loff=per spec VDD=5.0V VDD=10V VDD=15V		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V
High-Level Input Voltage	VIH	Ron=per spec, loff=per spec VDD=5.0V VDD=10V VDD=15V	3.5 7.0 11		3.5 7.0 11	2.75 5.50 8.25		3.5 7.0 11	- - -	V

PARAMETER	SYMBOL	TEST CONDITIONS	-55°C		25°C			125°C		UNIT
			MIN	MAX	MIN	TYP ^{*3}	MAX	MIN	MAX	
Input Leakage Current	I _{in}	V _{DD} =15V, V _{in} =0 or V _{DD}		±0.1		±10 ⁻⁵	±0.1		1.0	μA
Input Capacitance	C _{in}					5.0	7.5			pF
SWITCHES IN/OUT AND COMMONS OUT/IN –X,Y,Z(Voltages Referenced to V_{EE})										
Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	Channel On or Off	0	V _{DD}	0		V _{DD}	0	V _{DD}	V _{pp}
Recommended Static or Dynamic Voltage Across the Switch * ⁴ (Figure 3)	ΔV _{switch}	Channel On	0	600	0		600	0	300	mV
Output Offset Voltage	V _{oo}	V _{in} =0V, No Load				10				μV
ON Resistance	R _{on}	ΔV _{switch} ≤ 500mV * ⁴ V _{in} =V _{IL} or V _{IH} (Control), and V _{in} =0 to V _{DD} (Switch) V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		800 400 220		250 120 80	1050 500 280		1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		70 50 45		25 10 10	70 50 45		135 95 65	Ω
Off-Channel Leakage Current(Figure 8)	I _{off}	V _{DD} =15V, V _{in} =V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel		±100		±0.05	±100		±1000	nA
Capacitance, Switch I/O	C _{I/O}	Inhibit=V _{DD}				10				pF
Capacitance, Common O/I	C _{O/I}	Inhibit=V _{DD}				32				pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	Pins Not Adjacent Pins Adjacent				0.15 0.47				pF

*3. Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

*4. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS *5 (CL = 50 pF, TA = 25°C) (VEE ≤ Vss unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP*6	MAX	UNIT
Propagation Delay Times(Figure 4) Switch Input to Switch Output	tPLH,tPHL	RL=10k Ω VDD-VEE= 5.0, tPLH,tPHL=(0.17 ns/pF) CL+21.5 ns VDD-VEE=10, tPLH,tPHL=(0.08 ns/pF) CL+8.0 ns VDD-VEE=15, tPLH,tPHL=(0.06 ns/pF) CL+7.0 ns		30 12 10	75 30 25	ns
Propagation Delay Times(Figure 4) Inhibit to Output	tPHZ,tPLZ tPZH,tPZL	RL=10k Ω ,VEE=Vss Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level VDD-VEE= 5.0 VDD-VEE=10 VDD-VEE=15		300 155 125	600 310 250	ns
Propagation Delay Times(Figure 4) Control Input to Output	tPLN,tPHL	RL=10k Ω ,VEE=Vss VDD-VEE= 5.0 VDD-VEE=10 VDD-VEE=15		325 130 90	650 260 180	ns
Second Harmonic Distortion		RL=10k Ω , f=1kHz, Vin=5Vpp, VDD-VEE=10		0.07		%
Bandwidth (Figure 5)	BW	RL=1k Ω , Vin=1/2(VDD-VEE)p-p, CL=50pF, 20 Log (Vout/Vin)=-3dB, VDD-VEE=10		17		MHz
Off Channel Feedthrough Attenuation (Figure 5)		RL=1k Ω , Vin=1/2(VDD-VEE)p-p, Fin=30MHz, VDD-VEE=10		-50		dB
Channel Separation (Figure 6)		RL=1k Ω , Vin=1/2(VDD-VEE)p-p, fin=3.0MHz, VDD-VEE=10		-50		dB
Crosstalk ,Control Input to Common O/I (Figure 7)		R1=1k Ω , RL=10k Ω , Control tTLH=tTHL=20ns ,Inhibit=Vss, VDD-VEE=10		75		mV

*5. The formulas given are for the typical characteristics only at 25 °C.

*6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

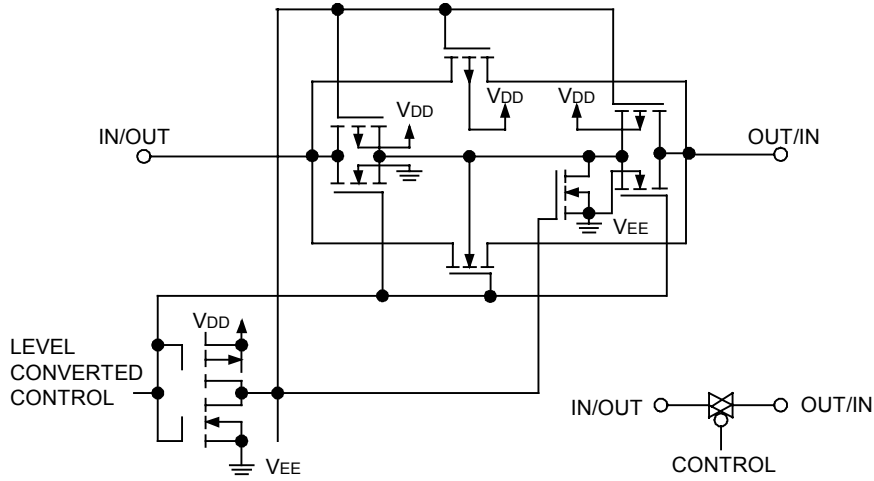


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs			ON Switches	
Inhibit	Select		Y0	X0
	B	A		
0	0	0	Y0	X0
0	0	1	Y1	X1
0	1	0	Y2	X2
0	1	1	Y3	X3
1	X	X	None	

* X=Don't Care

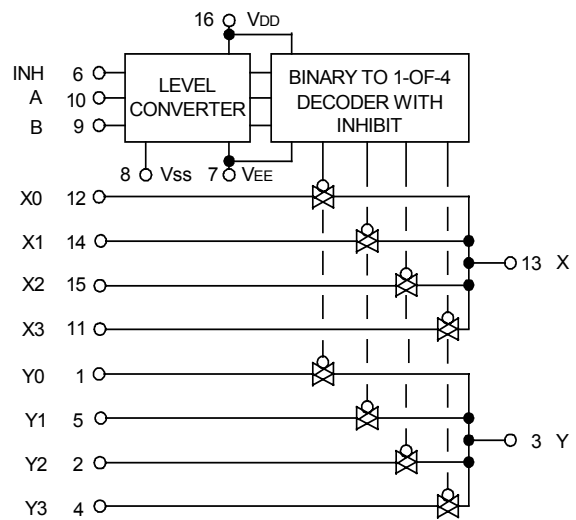


Figure 2. Functional Diagram

TEST CIRCUITS

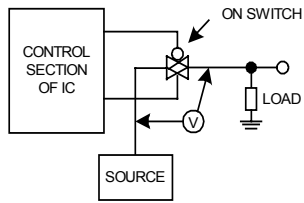


Figure 3. → ΔV Across Switch

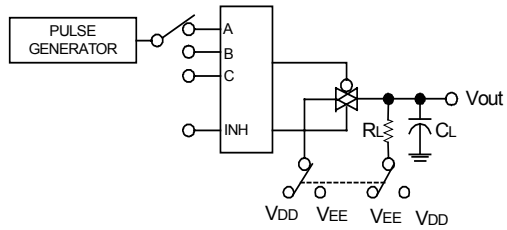


Figure 4. Propagation Delay Times, Control and Inhibit to Output

A,B, and C inputs used to turn ON or OFF the switch under test.

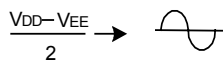
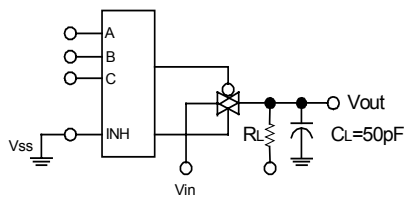


Figure 5. Bandwidth and Off-Channel Feedthrough Attenuation

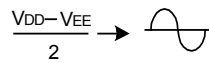
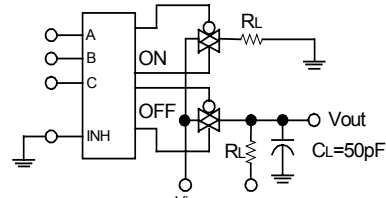


Figure 6. Channel Separation (Adjacent Channels Used For Setup)

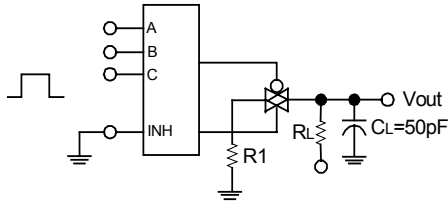


Figure 7. Crosstalk, Control Input to Common O/I

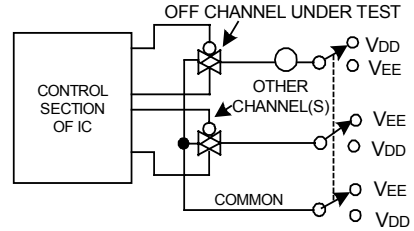


Figure 8. Off Channel Leakage

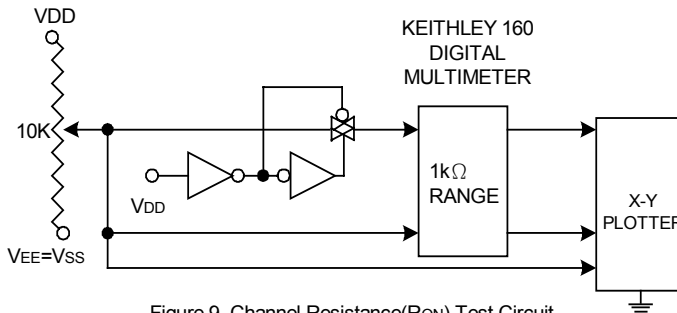
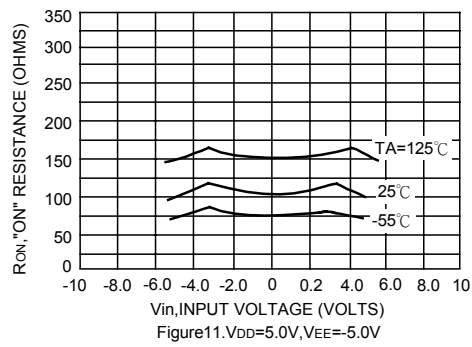
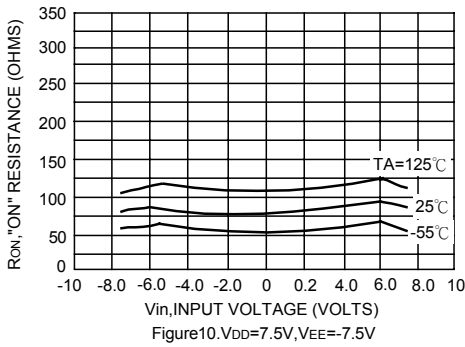


Figure 9. Channel Resistance(Ron) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS



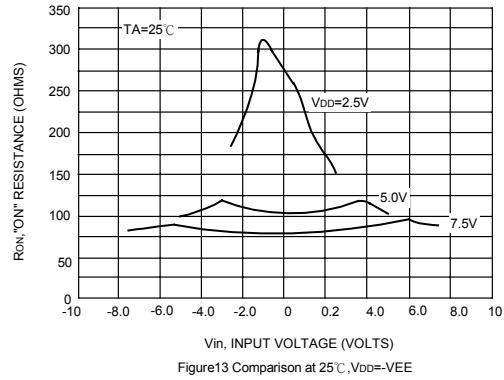
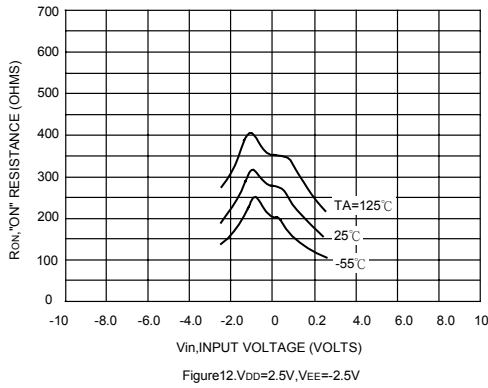


Figure A illustrates use of the on-chip level converter detailed in Figures 2. The 0 ~ 5 V Digital Control signal is used to directly control a 9 Vp-p analog signal.

The digital control logic levels are determined by VDD and VSS. The VDD voltage is the logic high voltage; the VSS voltage is logic low. For the example, VDD = + 5 V = logic high at the control inputs; VSS = GND = 0 V = logic low.

The maximum analog signal level is determined by VDD and VEE. The VDD voltage determines the maximum recommended peak above VSS. The VEE voltage determines the maximum swing below VSS. For the example, VDD - VSS = 5 V maximum swing above VSS; VSS - VEE = 5 V maximum swing below VSS. The example shows a ± 4.5 V signal which allows a 1/2 volt margin at each peak. If voltage transients above VDD and/or below VEE are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between VDD and VEE is 18.0 V. Most parameters are specified up to 15 V which is the recommended maximum difference between VDD and VEE.

Balanced supplies are not required. However, VSS must be greater than or equal to VEE. For example, VDD = + 10 V, VSS = + 5 V, and VEE = - 3 V is acceptable. See the Table below.

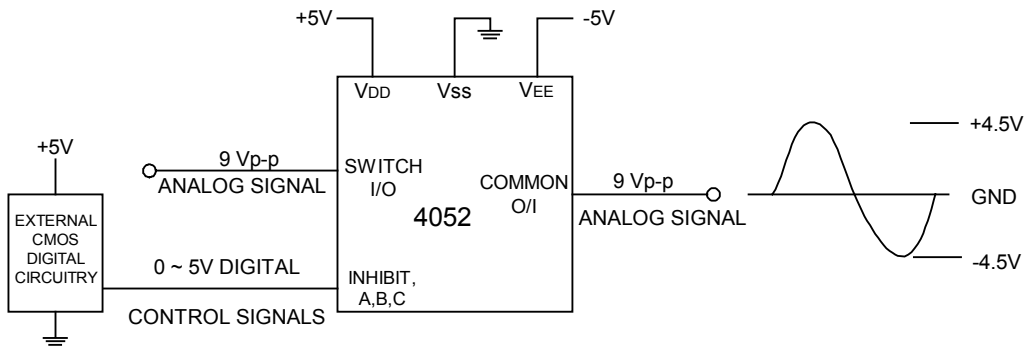


Figure A. Application Example

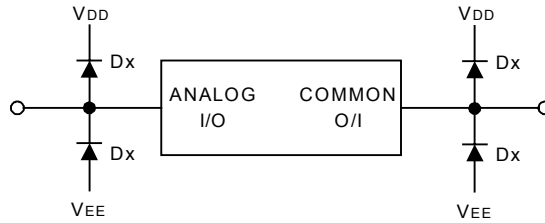


Figure B.External Germanium or Schottky Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

VDD IN VOLTS	VSS IN VOLTS	VEE IN VOITS	CONTROL INPUTS LOGIC HIGH/LOGIC LOW IN VOLTS	MAXIMUM ANALOG SIGNAL RANGE IN VOLTS
+8	0	-8	+8/0	+8 ~ -8=16Vp-p
+5	0	-12	+5/0	+5 ~ -12=17Vp-p
+5	0	0	+5/0	+5 ~ 0=5Vp-p
+5	0	-5	+5/0	+5 ~ -5=10Vp-p
+10	+5	-5	+10/+5	+10 ~ -5=15Vp-p